IN THE CLAIMS

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please **AMEND** claims 1, 4, 7 and 14-16 in accordance with the following:

1. (CURRENTLY AMENDED) A cache device set up in each of processors, interconnected to other cache devices in other processors and connected to a main memory, which comprises:

a cache memory wherein a part of data in the main memory is stored in one or more cache lines and a state tag ~~using~~used to manage data consistency is set up in each of the cache lines, and

OK TO ENTER - HBP 02/14/2005

a cache controller ~~for carrying out~~performing, as a pre-fetch protocol, a weak read operation that fails a pre-fetch request following a read request from one of the processors, ~~in a case that~~if at a time of generation of athe pre-fetch request, the state tags of other cache devices must be changed to read ~~following a read request from one of the processors~~ the data stored in the other cache devices ~~must be read by changing state tags of the other cache devices, weak read operation for causing failure in said pre-fetch request as a pre-fetch protocol~~.

2. (ORIGINAL) The cache device according to claim 1, wherein said cache memory distinguishes the stored data by a data-modified state (M), an exclusive state (E), a data-shared state (S) and an invalid state (I), each of which indicates validity of the state tag, and

said cache controller causes failure in said pre-fetch request when the data corresponding to the pre-fetch request stored in the other cache devices is in the data-modified state (M) or the exclusive state (E).

3. (ORIGINAL) The cache device according to claim 1, wherein said cache